Application Serial No. 06/555,426 is also a Continuation-in-Part of Serial No. 06/330,599 filed 12/14/81, now U.S. Patent No. 4,441,087; which is a Continuation of Serial No. 05/973,741 filed 12/28/78, now abandoned; which is a Continuation-in-Part of Serial No. 05/890,586 filed 03/20/78, now U.S. Patent No. 4,184,128.

Application Serial No. 06/178,107 is also a Continuation-in-Part of Serial No. 06/023,849 filed 03/26/79, now U.S. Patent No. 4,279,011.

IN THE CLAIMS

Claims 1-24 are continued and new claims 25-30 are added.

All the claims currently pending are provided by way of the document hereto attached and entitled AMENDED CLAIMS in Serial No. 07/717,860.

To cover the fee for the additional claims, a check (#4056) for $192.00 is attached hereto. (Applicant no longer qualifies as a Small Entity.)

REMARKS

Examiner rejected claims 1-24 under 35 USC 102e as being clearly anticipated by Stolz.

Applicant traverses these rejections for the following reasons.

(a) Applicant's invention, as defined by claims 1-24, is supported by the subject matter disclosed in Applicant's application Serial No. 06/973,741 filed 12/28/78; which subject matter has been maintained in unbroken continuity since that time.

Hence, the Stolz reference -- which has a priority date of 05/07/79 -- is not applicable as prior art against Applicant's claimed invention.

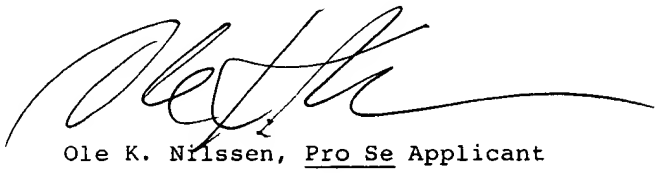
(b) Exemplary claim 1 includes:

"inverter means ... operative to provide an inverter voltage ... characterized by ... during each fundamental period, existing for a first period at a first substantially constant voltage level and for a second period at a second substantially constant voltage level ... the duration of the first period being substantively shorter than half the duration of the fundamental period".

This feature is neither disclosed nor suggested by Stolz.

Thus, even if Stolz were to have represented an appropriate prior art reference, it would not have anticipated the claimed invention.

If Examiner were to continue to hold that Stolz does disclose the above-identified feature from exemplary claim 1, Applicant requests of Examiner to point out exactly where and/or how does Stolz disclose such a feature. In this connection, it is important for Examiner to note that the waveforms of Stolz's Fig. 6 are not those of the output voltage of his inverter.



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AMENDED CLAIMS in Serial No. 07/717,860

1. (Amended) An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage being characterized by: (i) alternating periodically at a fundamental inverter frequency; (ii) having a fundamental period; (iii) during each fundamental period, existing for a first period at a first substantially constant voltage level and for a second period at a second substantially constant voltage level; (iv) the duration of the first period being substantially equal to that of the second period; (v) the duration of the first period being longer than one eighth [fourth] of the duration of the fundamental period; and (vi) the duration of the first period being substantively shorter than half of the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including an energy-storing inductor means and a gas discharge device.

2. The arrangement of claim 1 wherein the duration of the first period is shorter than half of the duration of the fundamental period by at least one tenth.

3. The arrangement of claim 1 wherein: (i) the duration of half the fundamental period is between 8 and 32 micro-seconds; and (ii) the duration of the first period is shorter than half of the fundamental period by at least 2 micro-seconds.

4. The arrangement of claim 1 wherein the inverter means includes at least one periodically conducting transistor.

5. (Amended) The arrangement of claim 4 wherein, during each fundamental period, the periodically conducting transistor conducts in a forward direction only during [for] a first conduction period; the first conduction period having a duration substantially shorter than the duration of the first period.

6. The arrangement of claim 5 wherein the periodically conducting transistor: (i) has an emitter and a collector; and (ii) when it indeed conducts in its forward direction, it conducts current directly between its emitter and collector without causing any substantial voltage drop thereacross.

7. The arrangement of claim 5 wherein, during each fundamental period, the period during which the periodically conducting transistor conducts in its forward direction is shorter than the first period by at least 2 micro-seconds.

8. The arrangement of claim 5 wherein: (i) each fundamental period includes a first transition period during which the inverter voltage changes from its first substantially constant voltage level to its second substantially constant voltage level; (ii) the periodically conducting transistor conducts in its forward direction during part of the first period; and (iii) the periodically conducting transistor does not conduct in its forward direction during most of the first transition period.

9. The arrangement of claim 1 wherein the inverter voltage changes between the first voltage level and the second voltage level at a substantially uniform rate.

10. The arrangement of claim 1 wherein the load means additionally includes a capacitor means connected across the inverter terminals.

11. (Amended) An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter means having at least one periodically conducting transistor; the inverter voltage being characterized by: (i) alternating periodically at a fundamental inverter frequency; (ii) having a fundamental period; (iii) during each fundamental period, existing for a first period at a first substantially constant voltage level and for a second period at a second substantially constant voltage level; (iv) the duration of the first period being substantially equal to that of the second period; (v) the duration of the first period being longer than one eighth [fourth] of the duration of the fundamental period; and (vi) the duration of the first period being shorter than half the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including an energy-storing inductor means and a gas discharge device; the load current flowing though the transistor, but only during a part of the first period.

12. (Amended) An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage being characterized by: (i) alternating periodically at a fundamental inverter frequency, (ii) having a fundamental period, (iii) during each fundamental period, existing for a first period at a first substantially constant voltage level and for a second period at a second substantially constant voltage level, (iv) the duration of the first period being substantially equal to that of the second period, (v) the duration of the first period being longer than one eighth [fourth] of the duration of the fundamental period, and (vi) the duration of the first period being shorter than half the duration of the fundamental period; the inverter means including a periodically conducting transistor, which conducts current in its forward direction only during part of the first period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including an energy-storing inductor means and a gas discharge device.

13. An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage having a fundamental period; the inverter means having a first periodically conducting transistor operative to conduct in its forward direction only during a first conduction period; the first conduction period having a duration substantially shorter than half the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including energy-storing inductor means and a gas discharge lamp.

14. The arrangement of claim 13 wherein the inverter means has a second alternatingly conducting transistor operative to conduct in its forward direction only during a second conduction period; the second conduction period having a duration substantially shorter than half the duration of the fundamental period.

15. The arrangement of claim 13 wherein the first conduction period has a duration shorter than one quarter of the duration of the fundamental period.

16. An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage having a fundamental period; the inverter means having a periodically conducting transistor; the transistor having a control terminal receptive of a control signal; the control signal being an alternating voltage operative during all of a first part of each fundamental period to cause the transistor to be conductive while during all of the remainder of each such fundamental period to cause the transistor to be non-conductive; the duration of the first part being substantially shorter than half the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including energy-storing inductor means and a gas discharge lamp.

17. The arrangement of claim 16 wherein the duration of the first part is about equal to or shorter than one fourth of of the duration of the fundamental period.

18. The arrangement of claim 16 wherein the inverter means includes a pair of transistors series-connected across the DC terminals.

19. The arrangement of claim 16 wherein a shunt diode is connected in parallel with the transistor.

20. The arrangement of claim 16 including means for controlling the duration of said first part.

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21. An electronic ballast for a gas discharge lamp, comprising:

a source operative to provide a power line voltage at a set of power line terminals;

rectifier means connected with the power line terminals and operative to provide a DC voltage at a set of DC terminals; and

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage being characterized by: (i) alternating periodically at a fundamental frequency; (ii) having a fundamental cycle period including a first and a second half-cycle; (iii) during its first half-cycle, existing for a first duration at a first substantially constant voltage level; (iv) during its second half-cycle, existing for a second duration at a second substantially constant voltage level; (v) the first duration being substantially equal to the second duration; (vi) the first duration being longer than one fourth of the duration of the first half-cycle; and (vii) the first duration being substantially shorter than half the duration of the fundamental cycle period.

22. The electronic ballast of claim 21 wherein a gas discarge lamp is indeed connected in circuit with the inverter terminals.

23. An electronic ballast for a gas discharge lamp, comprising:

a source operative to provide a power line voltage at a set of power line terminals;

rectifier means connected with the power line terminals and operative to provide a DC voltage at a set of DC terminals; and

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage having the following characteristics: (i) alternating periodically at a fundamental frequency; (ii) having a fundamental cycle period including a first and a second half-cycle, the complete fundamental cycle period being divided into 360 degrees; (iii) during its first half-cycle, existing for a first duration at a first substantially constant voltage level; (iv) during its second half-cycle, existing for a second duration at a second substantially constant voltage level; (v) the first duration being substantially equal to the second duration; (vi) the first duration being substantially equal shorter than 180 degrees.

24. The electronci ballast of claim 23 wherein: (i) the fundamental frequency is equal to, or higher than, about 10 kHz; and (ii) the first duration does not exceed 165 degrees.

25. An electronic ballast for a gas discharge lamp, comprising:

a source operative to provide a power line voltage at a set of power line terminals;

rectifier means connected with the power line terminals and operative to provide a DC voltage at a set of DC terminals; and

inverter means connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter terminals; the alternating inverter voltage having a fundamental period and an instantaneous magnitude that (i) during a first period, remains substantially constant at a negative level, (ii) during a second period, increases at a substantially constant rate, (iii) during a third period, remains substantially constant at a positive level, and (iv) during a fourth period, decreases at a substantially constant rate; the sum of the durations of the four periods being equal to the duration of the fundamental period; the duration of the first period being approximately equal to that of the third period; the duration of the first period being distinctly shorter than half the duration of the fundamental period.

26. The electronic ballast of claim 25 wherein the duration of the second period is about equal to, or longer than, one tenth the duration of the first period.

27. The electronic ballast of claim 25 wherein the absolute magnitude of the DC voltage is substantially higher than the peak absolute magnitude of the power line voltage.

28. The electronic ballast of claim 25 wherein the inverter is characterized by including an inductor and a capacitor connected together and being resonant at or near the fundamental frequency of the alternating inverter voltage.

29. The electronic ballast of claim 25 wherein the inverter includes means for controlling the frequency of the alternating inverter voltage.

30. The electronic ballast of claim 25 wherein the inverter is characterized by including: (i) a periodically conducting transistor having control input terminals; and (ii) a control signal source providing an alternating control signal to the control input terminals, the peak-to-peak magnitude of the control signal being substantially larger than twice the forward voltage drop of an ordinary semiconductor diode junction.